a first step of selecting one output terminal out of plural output terminals of a first memory element; and

a second step of connecting the selected output terminal of the first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein both said first step and said second step are performed on the basis of physical layout information.

2. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating a beeline distance on a substrate from each of said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum beeline distance to said scan data input terminal of said second memory element with said scan data input terminal of said second memory element.

5. (Amended) A method of wiring a semiconductor integrated circuit to include a

B2 scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum wire length with said scan data input terminal of said second memory element.

B3 8. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element; and

connecting one of aid output terminals having minimum fan-out with said scan data input terminal of said second memory element.

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11. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

a first step of selecting one output terminal out of plural output terminals of a first memory element; and

a second step of connecting the selected output terminal of the first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein both said first step and said second step are performed on the basis of physical timing information.

12. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element; and

connecting one of said output terminals of said first memory element having a minimum load capacitance with said scan data input terminal of said second

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memory element.

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15. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having a maximum driving ability and connecting said selected output terminal with said scan data input terminal of said second memory element.

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17. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

connecting one of said output terminals of said first memory element having a design margin larger than a predetermined value with said scan data input terminal of said second memory element, said design margin being obtained as a

B6 difference between one cycle time of a clock signal and propagation time required for a signal to travel from each of said output terminals of said first memory element to another memory element or an external output port.

B7 19. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having maximum delay time of a signal received at said scan data input terminal of said first memory element and connecting said selected output terminal with said scan data input terminal of said second memory element.

20. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of: